DLC Display Co., Limited

德爾西顯示器有限公司

MODEL No: DLC0049AZOG-W-1

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Record of Revision

Date	Revision No.	Summary
2014-08-17	1.0	Rev 1.0 was issued

1. Scope

This data sheet is to introduce the specification of DLC0049AZOG-W-1, passive matrix OLED module. It is composed of an OLED panel, driver ICs and FPC. The 0.49″ display area contains 64 x 32pixels.

2. Application

Digital equipments which need display, instrumentation, remote control, electronic product.
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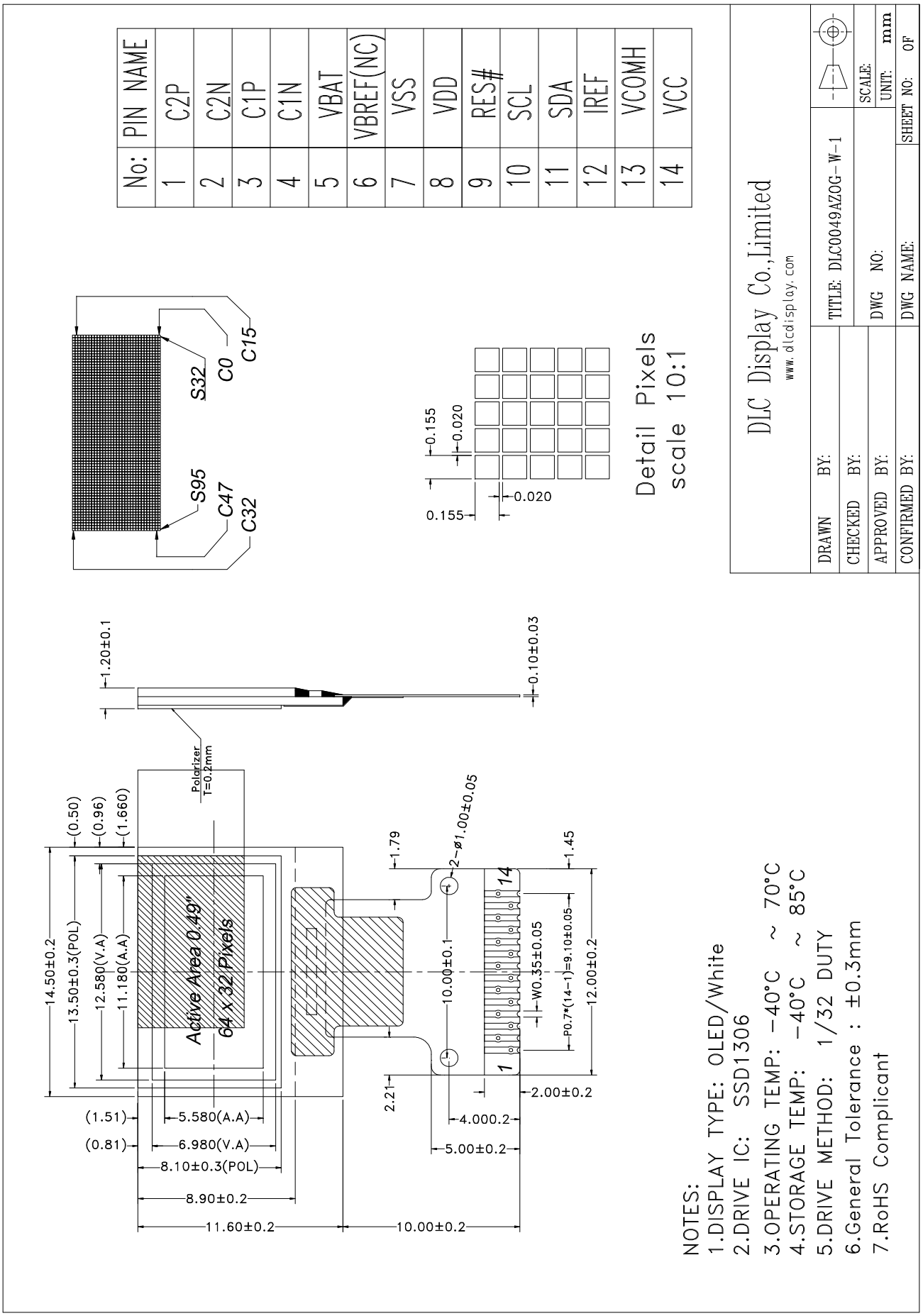
3. General Information

Item	Contents	Unit
Size	0.49	inch
Resolution	64 x 32	/
Display Color	White	
Interface	IIC	
Dot Size	0.155(W) x 0.155 (H)	mm
Pixel pitch	0.175(W) x 0.175 (H)	mm
Outline Dimension	14.5 x 11.6x 1.2	mm
Active Area	11.18 x 5.58	mm
Driver IC	SSD1306	
Drive Duty	1/32 Duty	/
Operating Temperature	-40℃~+70℃	
Storage Temperature	-40℃~＋85℃	

4. Outline Drawing



5. Interface signals

NO	Symbol	Type	Description
1	C2P	I	Positive Terminal of the Flying Inverting Capacitor Negative Terminal of the Flying Boost Capacitor The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
2	C2N		
3	C1P		
4	C1N		
5	VBAT	P	Power Supply for DC/DC Converter Circuit This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.
6	VBREF	P	NC
7	VSS	P	Ground of Logic circuit This is a ground pin. It also acts as a reference for the logic pins, It must be connected to external ground.
8	VDD	P	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.
9	RES#	I	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
10	SCL	I	IIC Bus Clock Signal The transmission if information in the I2C bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
11	SDA	I	IIC Bus data Signal This pin acts as a communication channel between the transmitter and the receiver.
12	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current lower than 12.5 A.
13	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
14	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.

6. Environment Conditions

6.1 Electrical Absolute max. ratings

Parameter	Symbol	MIN	MAX	Unit	Remark
Supply Voltage for Logic	VDD	-0.3	4.0	V	
Supply Voltage for Display	VCC	0	16.0	V	
Supply Voltage for DC/DC	VBAT	-0.3	4.3	V	

Note 1: All the above voltages are on the basis of “VSS = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

6.2 Environment Conditions

Item	Symbol	MIN	MAX	Unit	Remark
Operating Temperature	TOPR	-40	70	℃	
Storage Temperature	TSTG	-40	85	℃	

Note1: The defined temperature ranges do not include the polarizer.
The maximum withstood temperature of the polarizer should be 80℃.

7. Electrical Specifications

7.1 Electrical characteristics

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Supply Voltage for Logic	VDD	1.65	2.8	3.3	V	
Supply Voltage for Display (Supplied Externally)	VCC	7	-	9.0	V	Note 1 (Internal DC/DC Disable)
Supply Voltage for DC/DC	VBAT	3.5	-	4.2	V	
Supply Voltage for Display (Generated by Internal DC/DC)	VCC	7	7.25	7.5		Note 2 (Internal DC/DC Enable)
High-level Input Voltage	VIH	0.8xVDD	-	-	V	Iout=100uA, 3.3MHz
Low-level Input Voltage	VIL	-	-	0.2xVDD	V	Iout=100uA, 3.3MHz
High-level Output Voltage	VOH	0.9xVDD	-		V	Iout=100uA, 3.3MHz
Low-level Output Voltage	VOL	-	-	0.1xVDD	V	Iout=100uA, 3.3MHz
Operating Current for VDD	IDD	-	180	300	A	
Operating Current for VCC (VCC Supplied Externally)	ICC	-	5	10	mA	Note 3
Operating Current for VBAT (VCC Generated by Internal DC/DC)	IBAT	-	10	15	mA	Note 4
Sleep Mode Current for VDD	$I_{DD, SLEEP}$	-	1	5	A	
Sleep Mode Current for VCC	$I_{CC, SLEEP}$	-	2	10	A	

Note 1 & 2: Brightness (Lbr) and Supply Voltage for Display (VCC) are subject to the change of the panel characteristics and the customer's request.

Note 3: VDD = 2.8V, VCC = 7.25V, 100% Display Area Turn on.

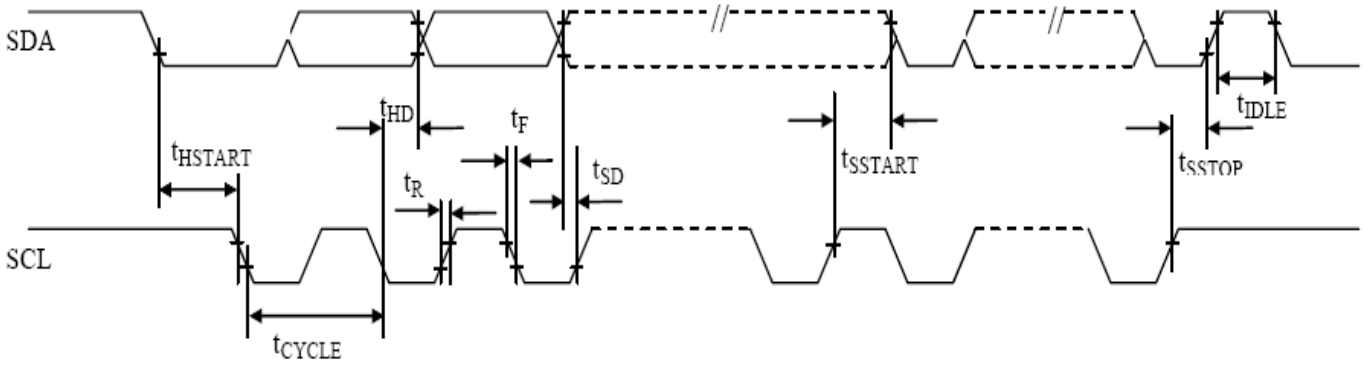
Note 4: VDD = 2.8V, VCC = 7.25V, 100% Display Area Turn on.

8. AC Timing/Functional Specification

8.1 I^2C Interface Timing Characteristics

Symbol	Description	Min	Max	Unit
t_{cyde}	Clock Cycle Time	2.5	-	s
t_{HSTART}	Start Condition Hold Time	0.6	-	s
t_{HD}	Data Hold Time (for "SDAOUT" Pin)	0	-	ns
	Data Hold Time (for "SDAIN" Pin)	300	-	ns
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	s
t_{SSTOP}	Stop Condition Setup Time	0.6	-	s
t_R	Rise Time for Data and Clock Pin	-	300	ns
t_F	Fall Time for Data and Clock Pin	-	300	ns
tIDLE	Idle Time before a New Transmission can Start	1.3	-	s

* (VDD - VSS = 1.65V to 3.3V, Ta = 25°C)

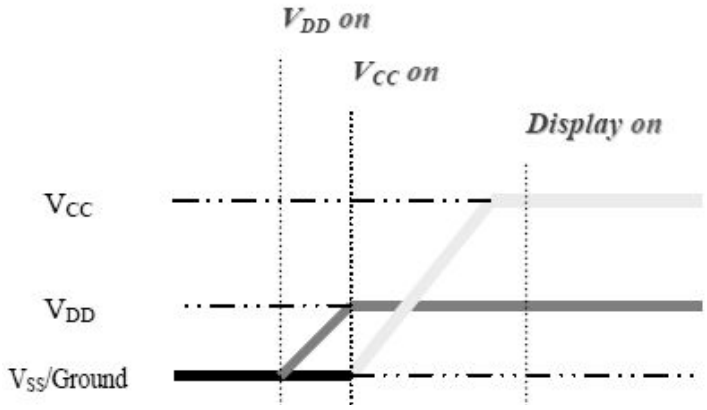


8.2 Power down and Power up Sequence

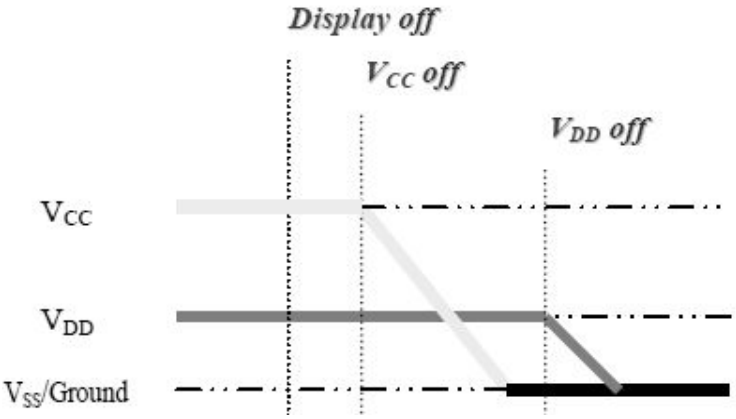
To protect OELD panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

8.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VCC/VBAT
6. Delay 100ms (When VCC is stable)
7. Send Display on command



8.2.2 Power down Sequence:
1. Send Display off command
2. Power down VCC/VBAT
3. Delay 100ms (When VCC/VBAT is reach 0 and panel is completely discharges)
4. Power down VDD



Note :
1) Since an ESD protection circuit is connected between VDD and VCC inside the driver IC, VCC becomes lower than VDD whenever VDD is ON and VCC is OFF.
2) VCC / VBAT should be kept float (disable) when it is OFF.
3) Power Pins (VDD, VCC, VBAT) can never be pulled to ground under any circumstance.
4) VDD should not be power down before VCC / VBAT power down.

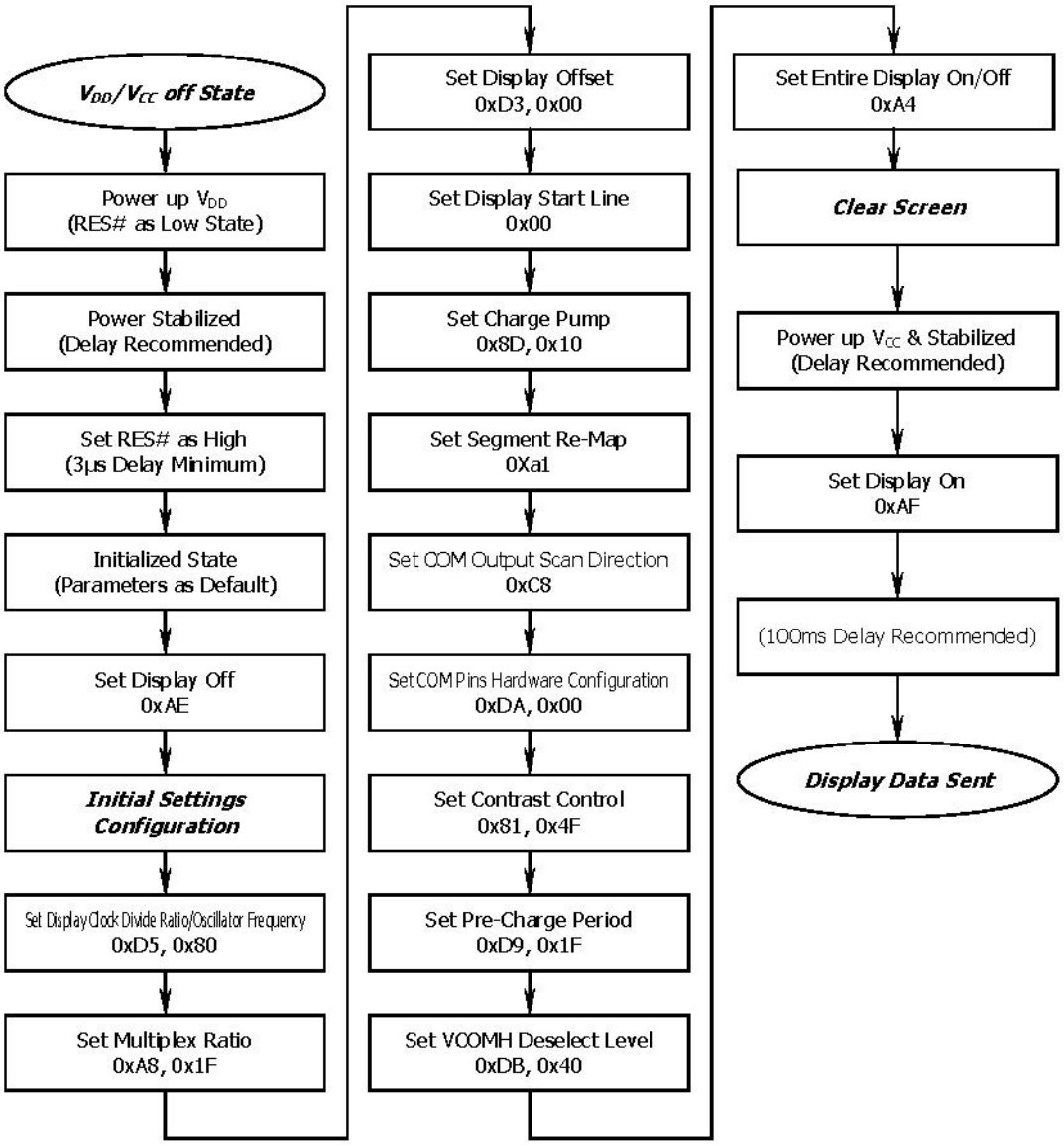
8.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:
1. Display is OFF
2. 64x32 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

8.4 Actual Application Example

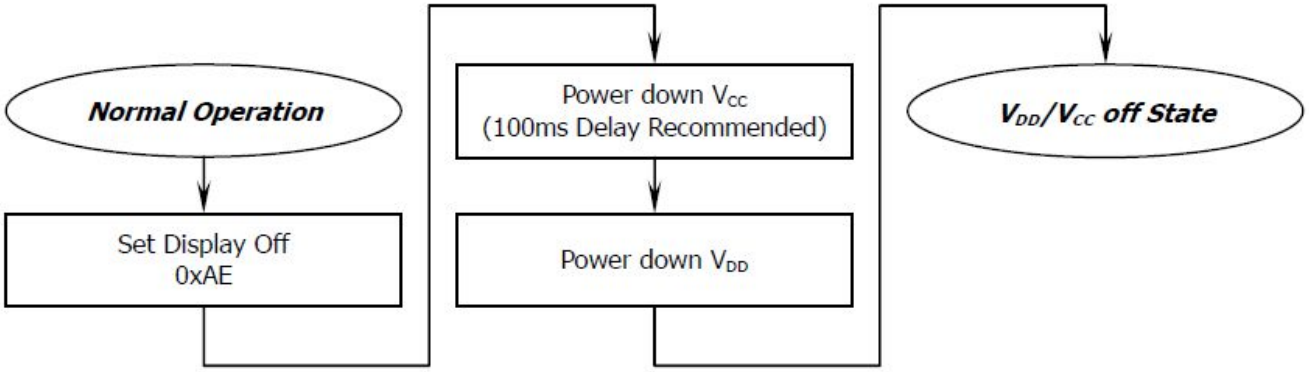
8.4.1 VCC Supplied Externally

<Power up Sequence>

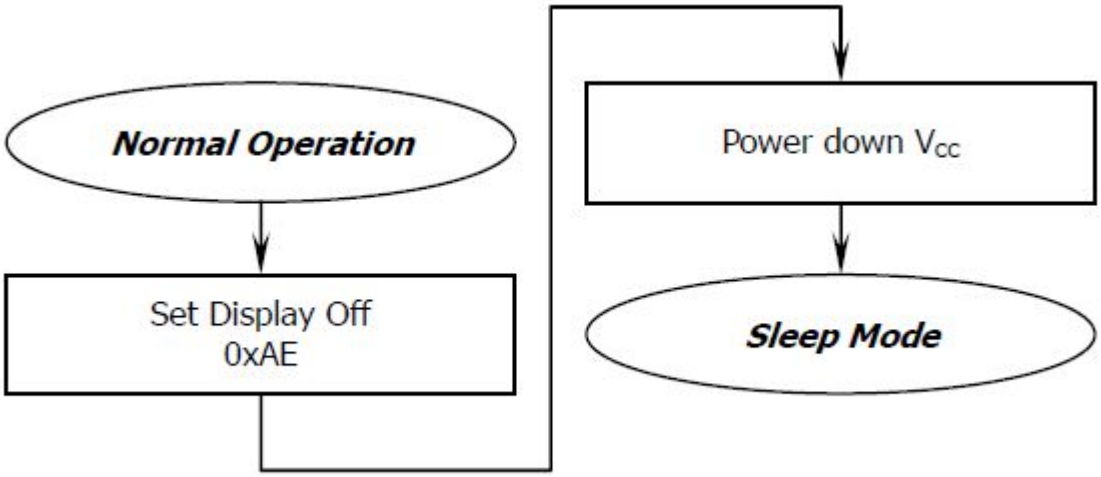


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

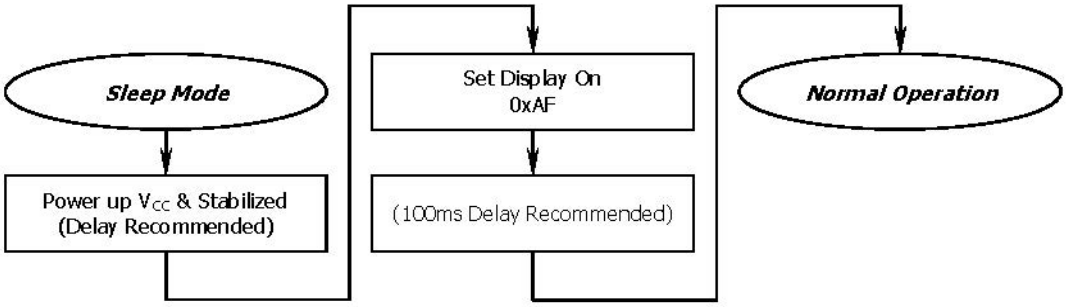
<Power down Sequence>



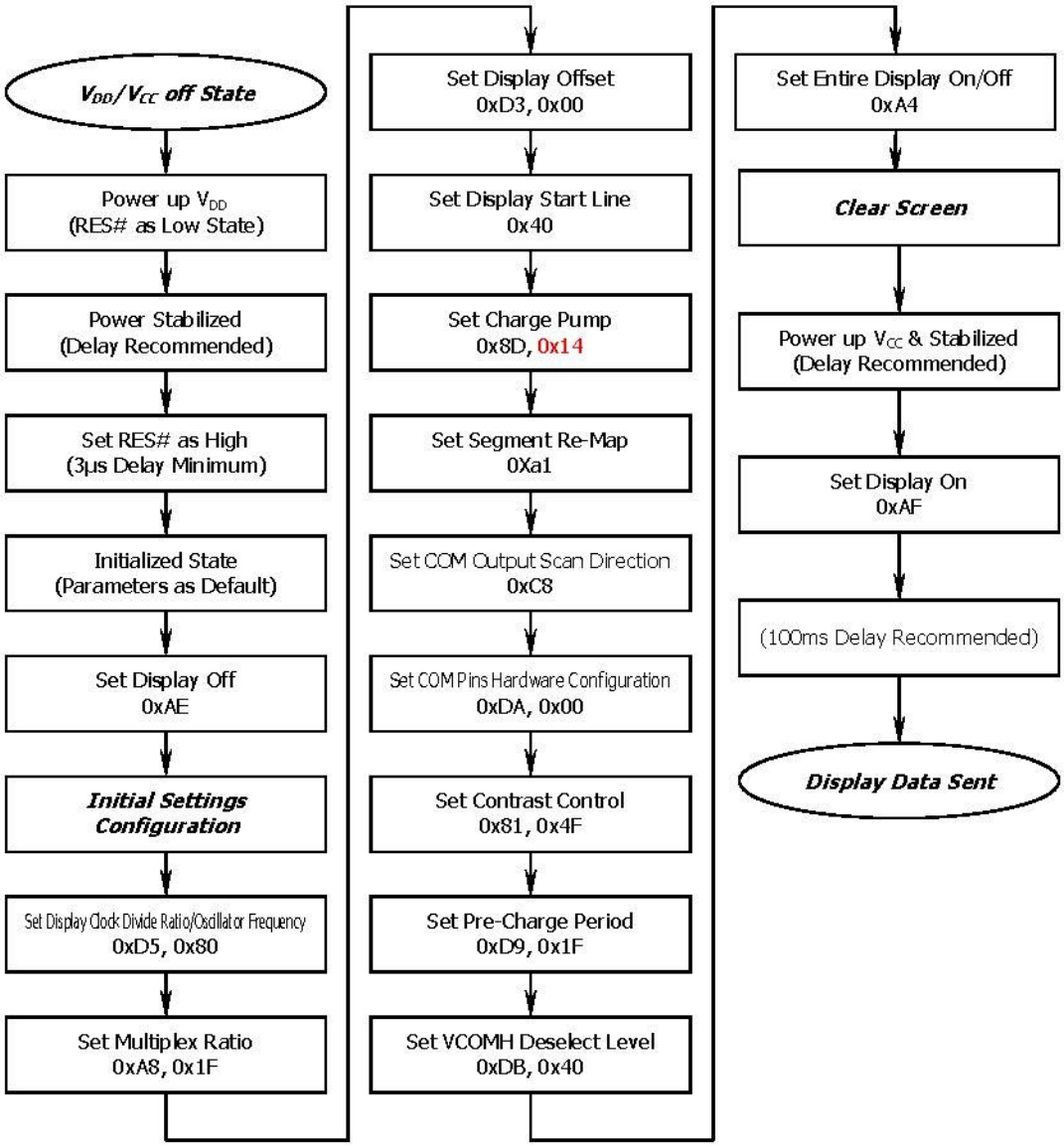
<Entering Sleep Mode>



<Exiting Sleep Mode>

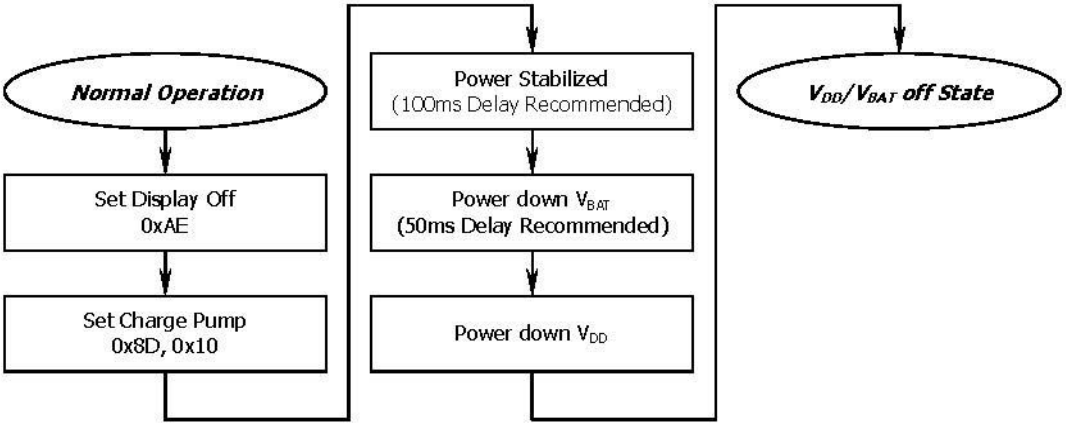


8.4.2 VCC Generated by Internal DC/DC Circuit
<Power up Sequence>

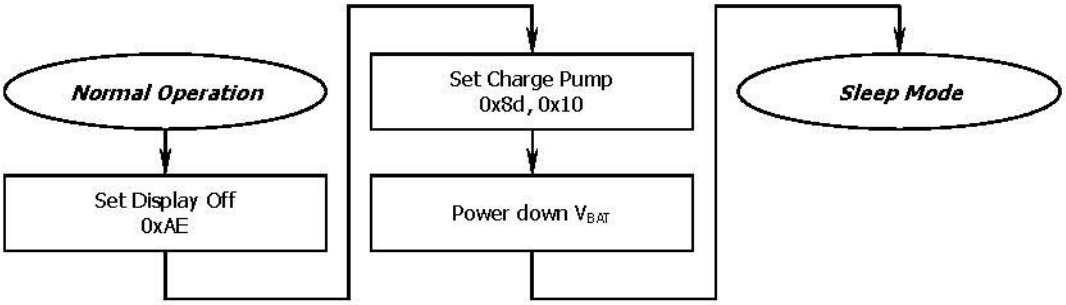


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

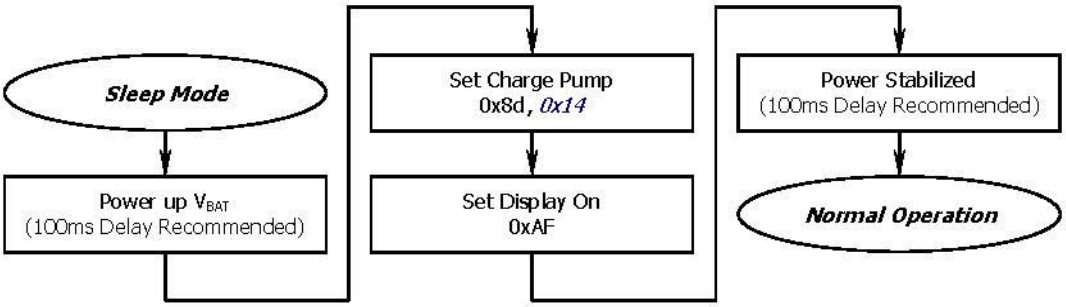
<Power down Sequence>



<Entering Sleep Mode>

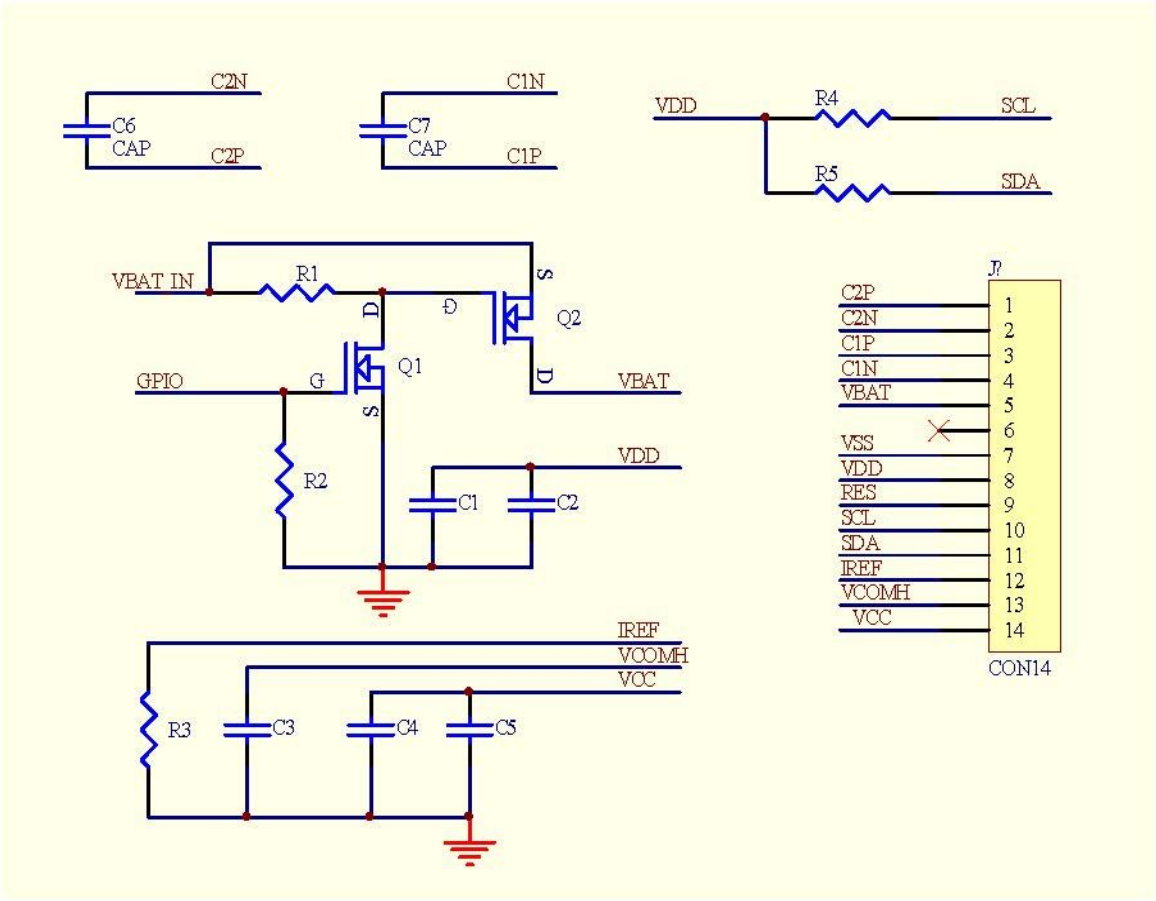


<Exiting Sleep Mode>



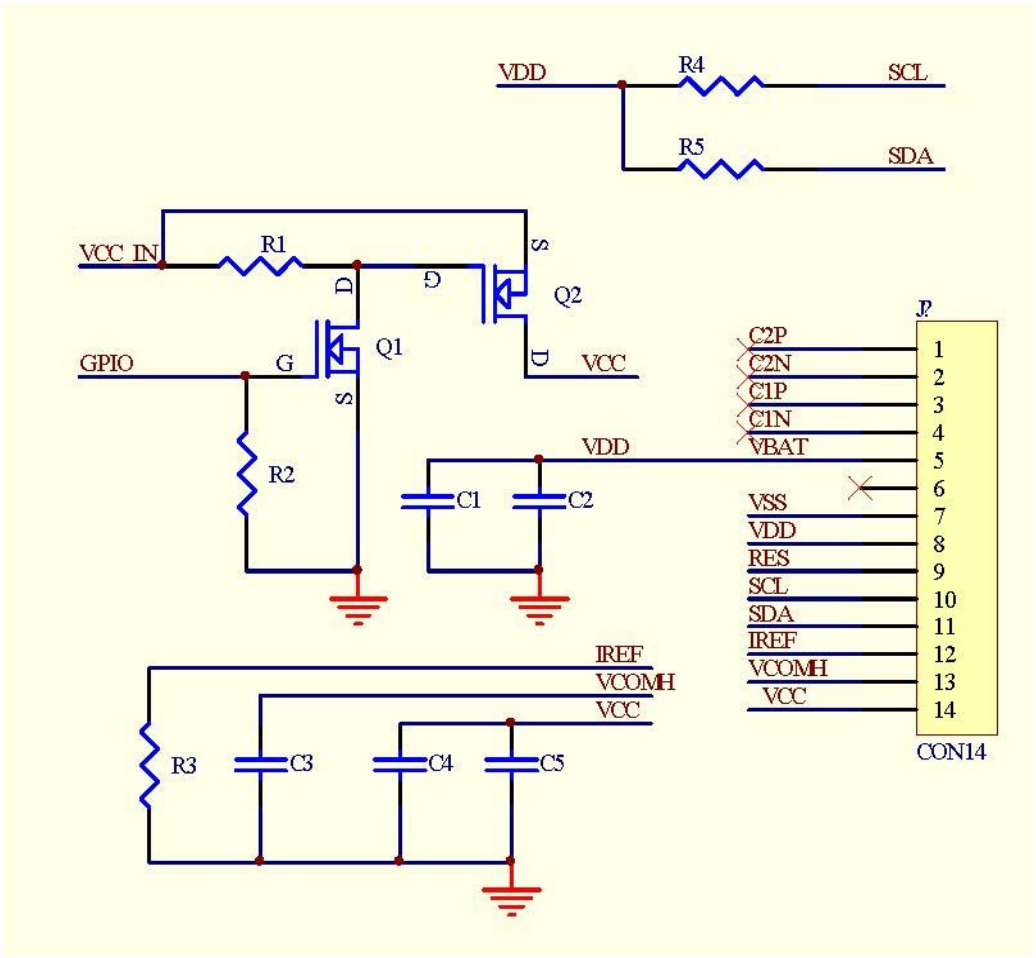
8.5 I²C Interface

8.5.1 I²C Interface with Internal Charge Pump



Recommended Components:
C1,: 0.1μF / 6.3V, X5R
C2: 4.7μF / 6.3V, X5R
C3: 2.2μF/ 16V, X7R
C4: 4.7μF / 16V, X7R
C5: 0.1μF / 16V, X7R
C6,C7: 1μF / 16V, X7R
R3: 560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1: 47kΩ
R4, R5: 4.7kΩ
Q1: FDN338P
Q2: FDN335N
Notes:
VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.
VBAT_in: 3.5~4.2V

8.5.2 I²C Interface with External VCC



Recommended Components:
C1,: 0.1µF / 6.3V, X5R
C2: 4.7µF / 6.3V, X5R
C3: 2.2µF/ 16V, X7R
C4: 4.7µF / 16V, X7R
C5: 0.1µF / 16V, X7R
R3: 560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1: 47kΩ
R4, R5: 4.7kΩ
Q1: FDN338P
Q2: FDN335N
Notes:
VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.
VCC_in: 7~7.5V

9. Optical Specification

Ta=25℃

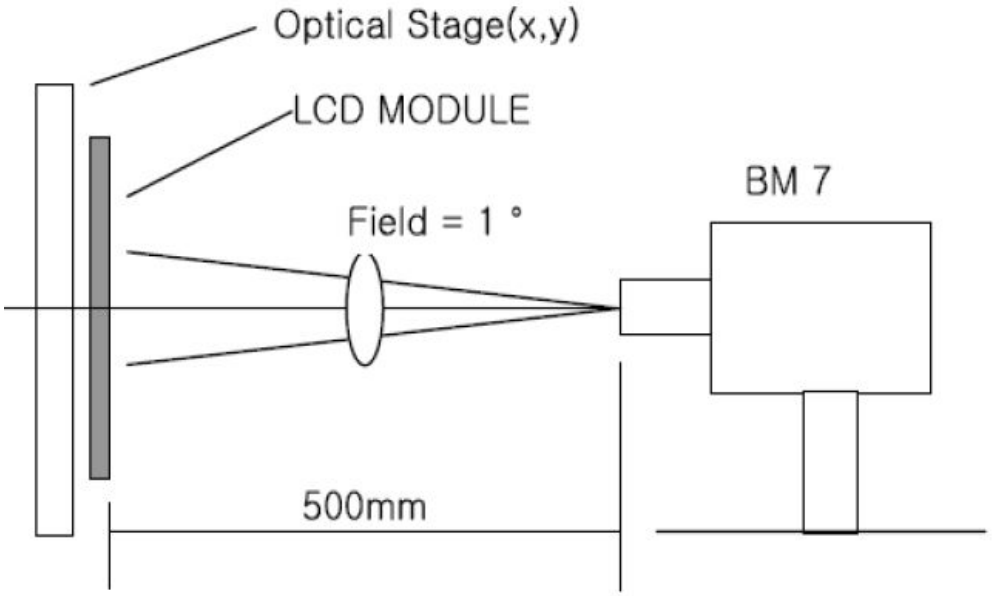
Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
Contrast Ratio		CR	θ=0°	2000		-		Note1 Note2
View Angles			--	-	Free	-	Degree	Note 3
Chromaticity	White	x	θ=0°	0.28	0.32	0.36		Note4, Note1
		y		0.31	0.35	0.39		
Luminance		L		160	180	-	cd/m²	Note1 Note5

*Optical measurement taken at VDD = 2.8V, VCC = 7.25V

Note 1: Definition of optical measurement system.

Temperature = 25℃(±3℃)

LED back-light: ON, Environment brightness < 150 lx

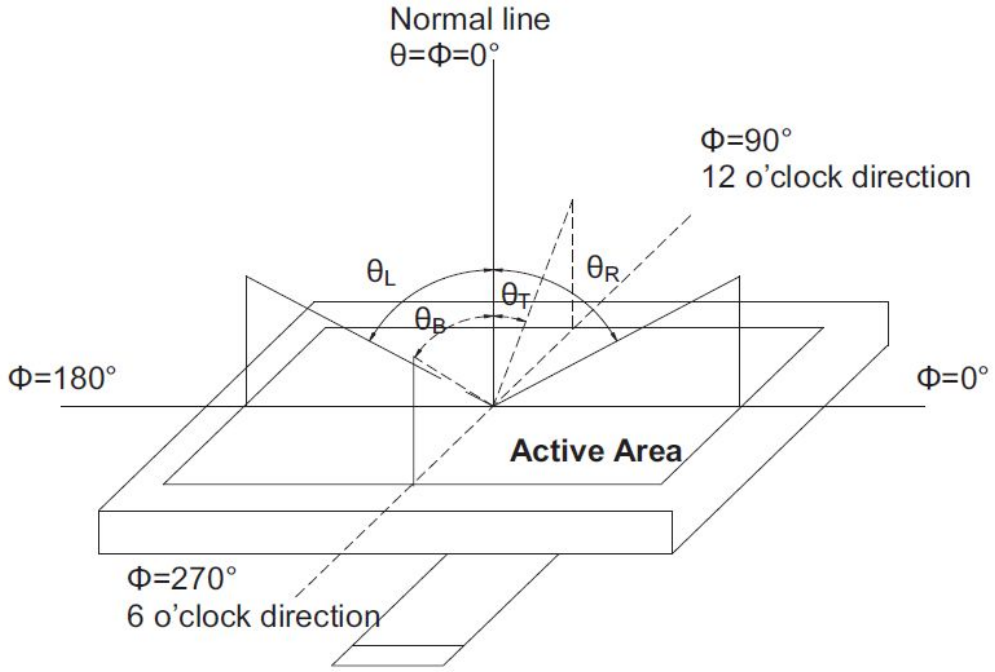


Note 2: Contrast ratio is defined as follow:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

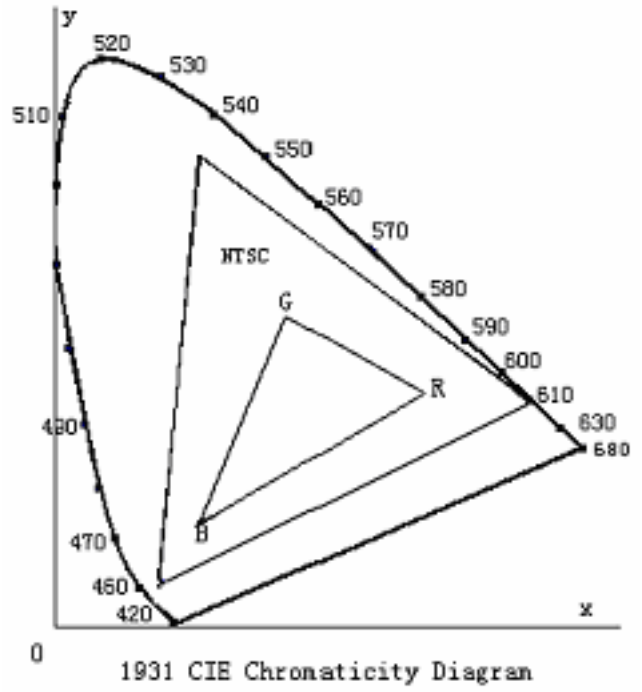
Note 3: Viewing angle range is defined as follow:

Viewing angle is measured at the center point of the LCD.



Note 4: Color chromaticity is defined as follow: (CIE1931)

Color coordinates measured at center point of LCD.



$$S = \frac{\text{area of RGB triangle}}{\text{area of NTSC triangle}} \times 100\%$$

Note 5: Luminance is defined as follow:

Luminance is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

10. Environmental / Reliability Tests

No	Test Item	Condition	Judgment criteria
1	High Temp Operation	Ts=+70℃, 120hrs	Per table in below
2	Low Temp Operation	Ta=-40℃, 120hrs	Per table in below
3	High Temp Storage	Ta=+85℃, 120hrs	Per table in below
4	Low Temp Storage	Ta=-40℃, 120hrs	Per table in below
5	High Temp & High Humidity Storage	Ta=+60℃, 90% RH 120 hours	Per table in below (polarizer discoloration is excluded)
6	Thermal Shock (Non-operation)	-40℃ 30 min~+70℃ 30 min, Change time:5min, 10 Cycles	Per table in below
7	ESD (Operation)	C=150pF, R=330Ω，5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times;	Per table in below
8	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z.	Per table in below
9	Shock (Non-operation)	60G 6ms, ±X,±Y,±Z 3times, for each direction	Per table in below
10	Package Drop Test	Height:80 cm, 1 corner, 3 edges, 6 surfaces	Per table in below

INSPECTION	CRITERION(after test)
Appearance	No Crack on the FPC, on the OLED Panel
Alignment of OLED Panel	No Bubbles in the OLED Panel No other Defects of Alignment in Active area
Electrical current	Within device specifications
Function / Display	No Broken Circuit, No Short Circuit or No Black line No Other Defects of Display

11. Precautions for Use of OLED Modules

11.1 Safety

The liquid crystal in the OLED is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

11.2 Handling

A. The OLED and touch panel is made of plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.
B. Do not handle the product by holding the flexible pattern portion in order to assure the reliability
C. Transparency is an important factor for the touch panel. Please wear clear finger sacks, gloves and mask to protect the touch panel from finger print or stain and also hold the portion outside the view area when handling the touch panel.
D. Provide a space so that the panel does not come into contact with other components.
E. To protect the product from external force, put a covering lens (acrylic board or similar board) and keep an appropriate gap between them.
F. Transparent electrodes may be disconnected if the panel is used under environmental conditions where dew condensation occurs.
G. Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in IC malfunctions.
H. To prevent such IC malfunctions, your design and mounting layout shall be done in the way that the IC is not exposed to light in actual use.

11.3 Static Electricity

A. Ground soldering iron tips, tools and testers when they are in operation.
B. Ground your body when handling the products.
C. Power on the OLED module before applying the voltage to the input terminals.
D. Do not apply voltage which exceeds the absolute maximum rating.
E. Store the products in an anti-electrostatic bag or container.

11.4Storage

A. Store the products in a dark place at +25℃±10℃ with low humidity (40% RH to 60% RH). Don't expose to sunlight or fluorescent light.
B. Storage in a clean environment, free from dust, active gas, and solvent.

11.5 Cleaning

A. Do not wipe the touch panel with dry cloth, as it may cause scratch.
B. Wipe off the stain on the product by using soft cloth moistened with ethanol. Do not allow ethanol to get in between the upper film and the bottom glass. It may cause peeling issue or defective operation. Do not use any organic solvent or detergent other than ethanol.

11.6 Cautions for installing and assembling

Bezel edge must be positioned in the area between the Active area and View area. The bezel may press the touch screen and cause activation if the edge touches the active area. A gap of approximately 0.5mm is needed between the bezel and the top electrode. It may cause unexpected activation if the gap is too narrow. There is a tolerance of 0.2 to 0.3mm for the outside dimensions of the touch panel and tail. A gap must be made to absorb the tolerance in the case and connector.